

Holonic Simulation of a Design System for Performance Analysis

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HoloMAS 2007
September 2007

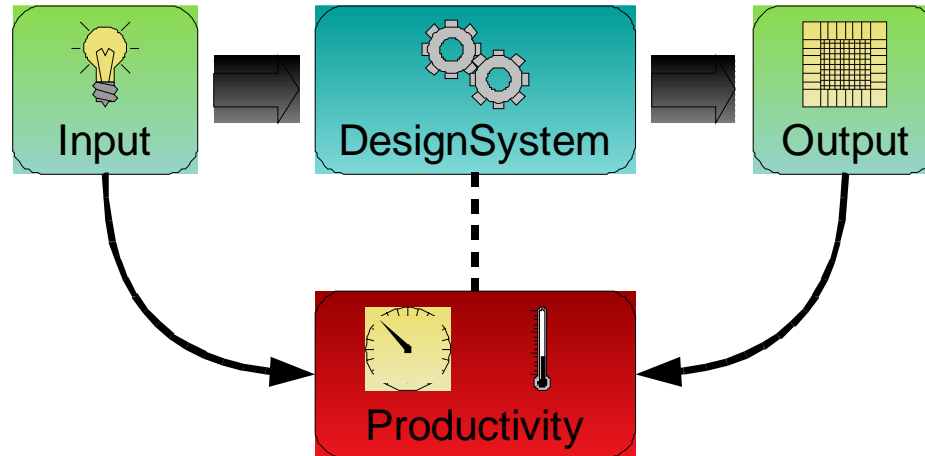


Overview



- The Problem
- Our Project
- Our Approach
- Simulation
 - Planning
 - Execution
 - Events
- Assessment
- Conclusions

The Problem



- Calculate Performance Indicators from Inputs and Outputs
- Current methods use a kind of black-box model for the Design System
- No reasons given for results, no justification of results
- No hints to improvements

- government funded joint project of
 - AMD
 - Cadence Design Systems
 - Infinion
 - Robert Bosch
 - + subcontractors

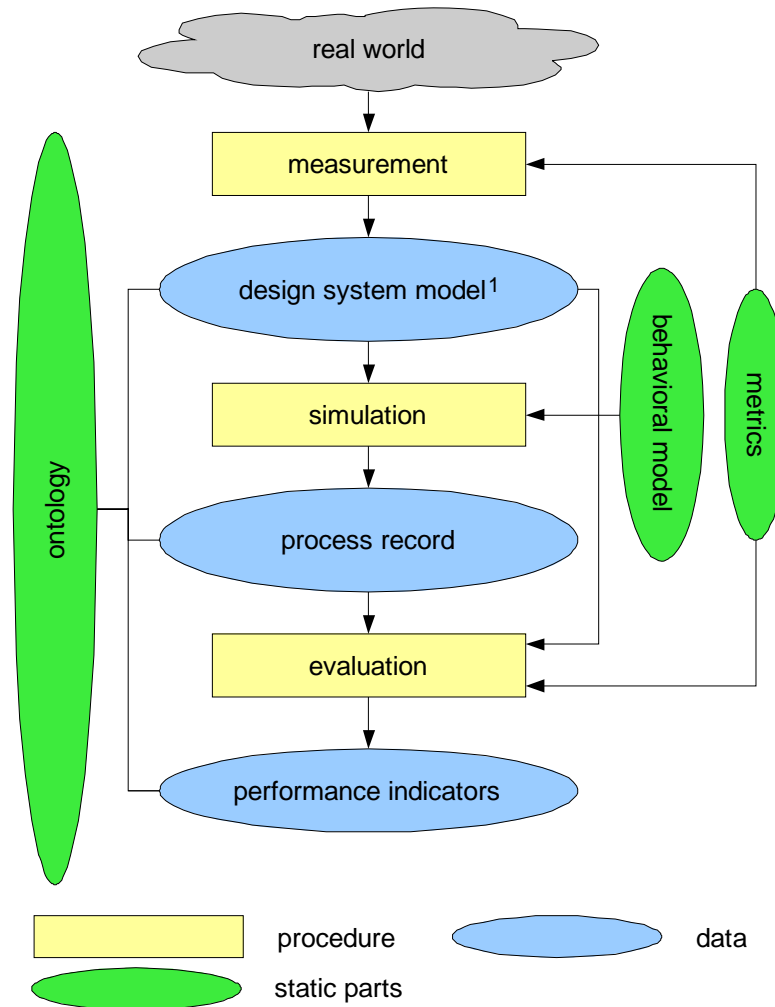
- Aims
 - Assessment of Productivity (and other KPIs) of Hardware Design Systems
 - Suggesting Improvements to Design Processes

Our Aims



- More Detailed, Comprehensible Assessment of the Design Process
- Zoom-In on Design Steps, Design Phases and/or Parts of the Design
- Find Weak Spots
- Predict Effect of changes/improvements
- Help Planning and Predicting Future Projects

Our Approach



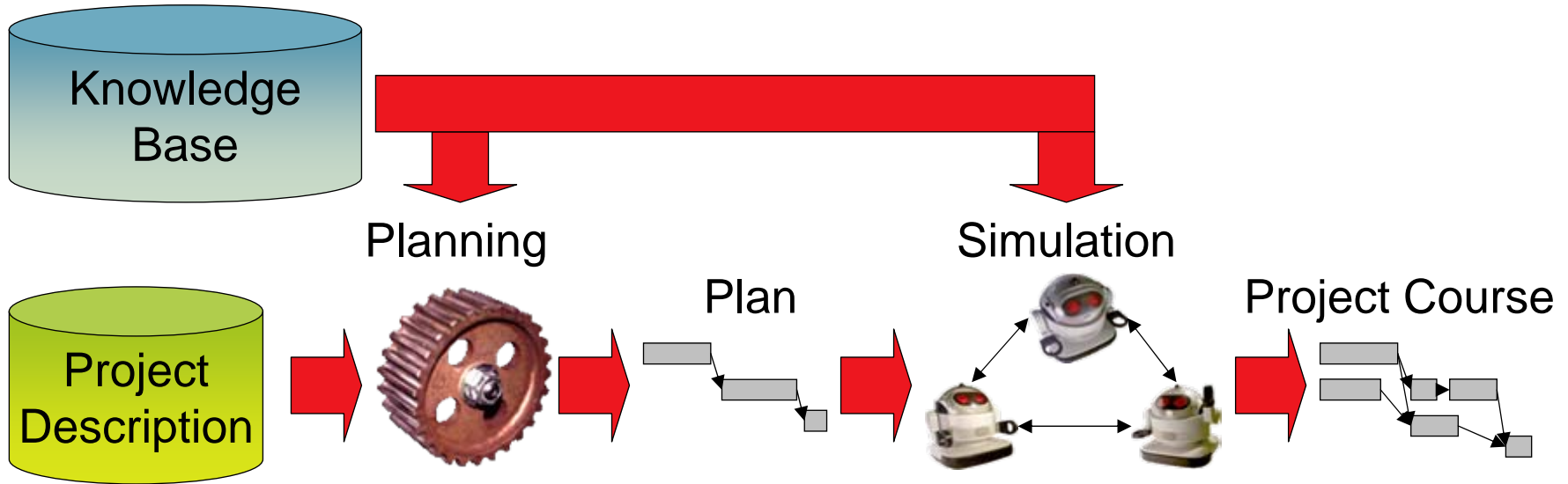
¹ the model contains the parameters in its instances

Demonstrator – System Description

The screenshot displays the CADENCE Project Planning Expert System interface. The main window is titled "CDN_MP3Flash 1 - System Description". It shows a hierarchical tree view of the project components and a corresponding table of their properties.

Name	Type	Initial State	Desired State	Complexity
CDN_MP3Flash 1			GDSII	
Toplevel	Mixed Digital	Specification		5.69
Audio OUT	Mixed Digital	Specification		1.50
Audio Amp	Analog	Specification		1.00
Audio DAC	Analog	LIB Description, RTL Shell, Macro Descriptio...		1.00
Audio Digital	Digital	Specification		1.19
Testbench of Audio OUT	Testbench	Specification		0.30
VR for Audio OUT	FunctionalVR	Specification		0.30
Boot ROM	Analog	LIB Description, RTL Shell, Macro Descriptio...		1.00
Clock Control	Digital	Specification		0.66
Testbench of Clock Control	Testbench	Specification		0.20
VR for Clock Control	FunctionalVR	Specification		0.20
FlashROM IF	Digital	Testplan, Specification, Verified RTL, Initial...		0.50
JTAG TAP	Digital	Testplan, Specification, Verified RTL, Initial...		0.50
MEM IF	Digital	Specification		0.73
RISC CPU	Digital	Testplan, Specification, Verified RTL, Initial...		2.00
SRAM	Analog	Testplan, LIB Description, Macro Descriptio...		1.00
USB Interface	Mixed Digital	Testplan, Specification, Verified RTL, Initial...		1.50
USB Digital	Digital	Testplan, Specification, Verified RTL, Initial...		1.00
USB PHY	Analog	LIB Description, RTL Shell, Macro Descriptio...		1.00
USB SRAM	Analog	LIB Description, RTL Shell, Macro Descriptio...		1.00
Wishbone Bus	Digital	Testplan, Specification, Verified RTL, Initial...		0.50
DRC Runset	PhysicalVR	DRC Runset		1.00
LVS Runset	LogicalVR	LVS Runset		1.00
Testbench of Toplevel	Testbench	Specification		1.00
VR for Toplevel	FunctionalVR	Specification		1.00

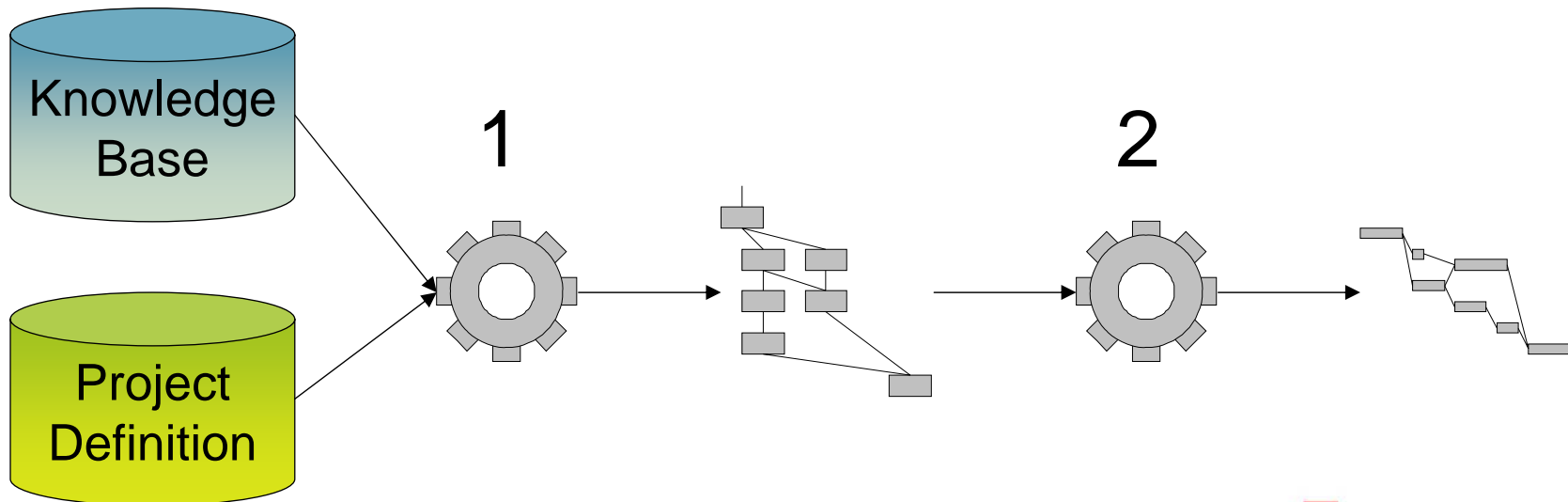
Simulation Overview



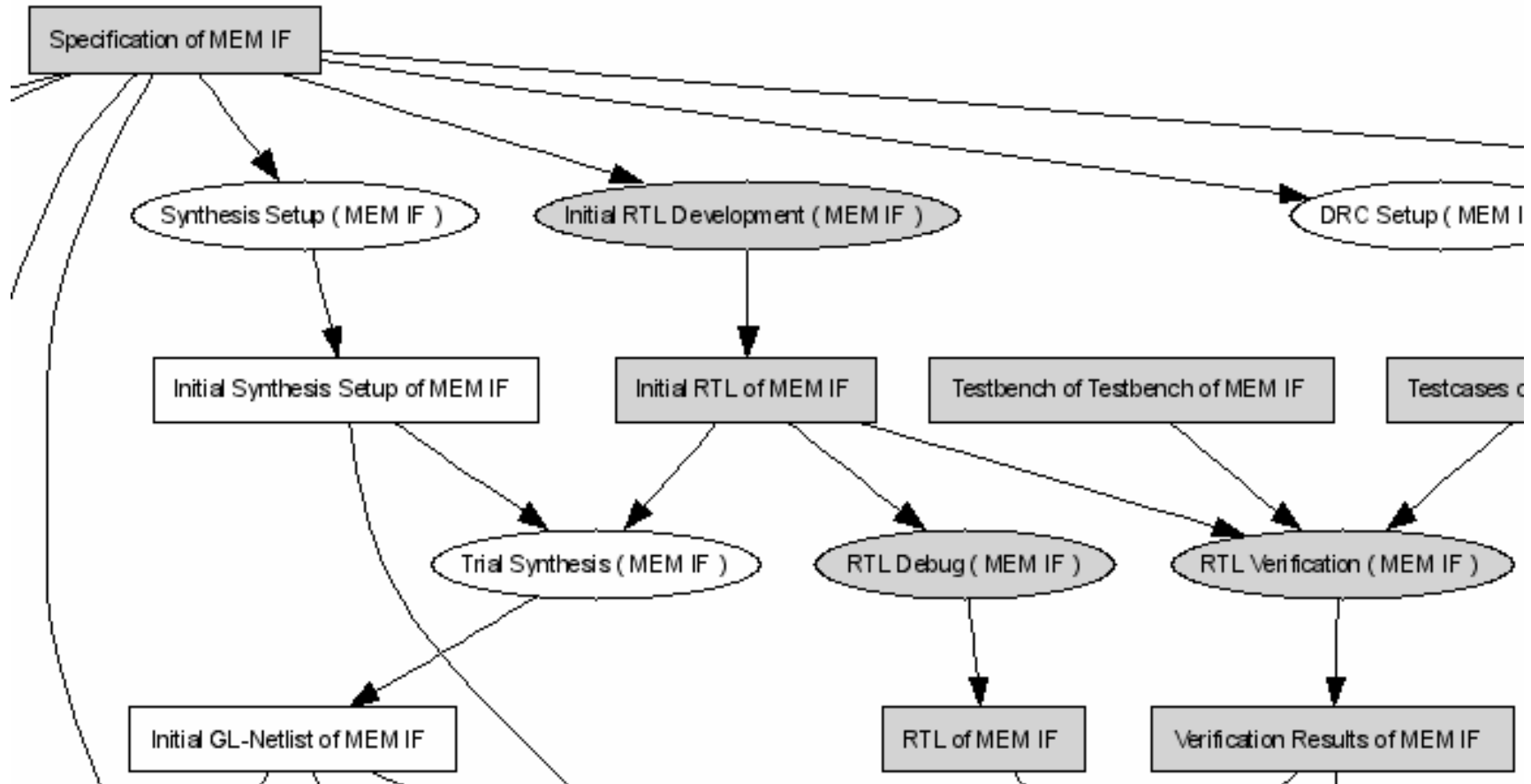
- Create a course-grain plan based on the knowledge and project description
- Simulate plan to test feasibility and find possible problems

Simulation – Planning

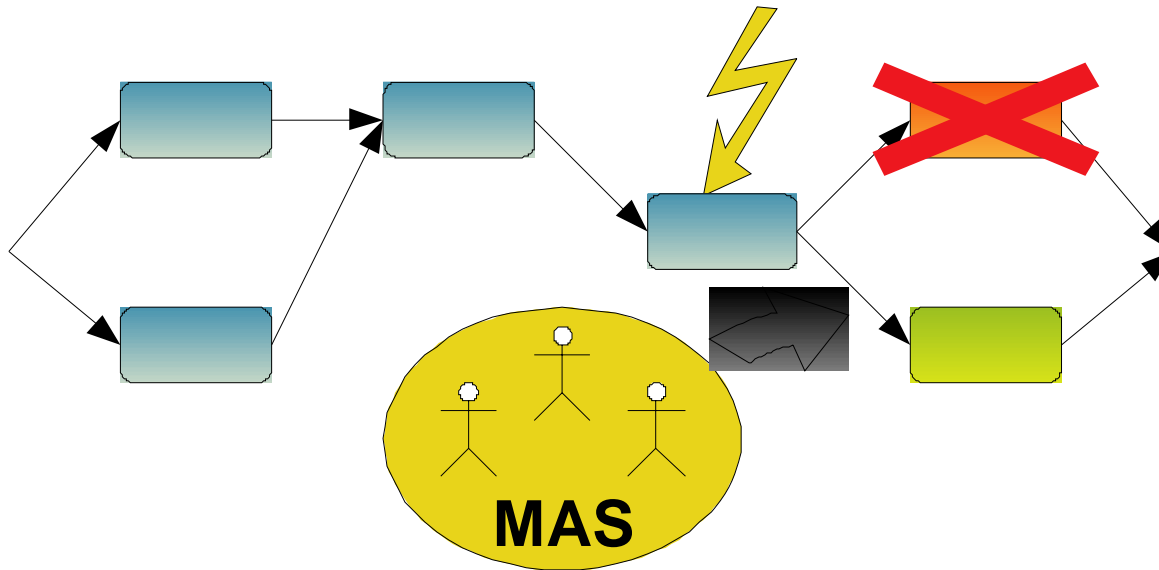
1. Generate a Work-Breakdown-Structure
2. Assign Resources and Schedule



WBS Generation Example

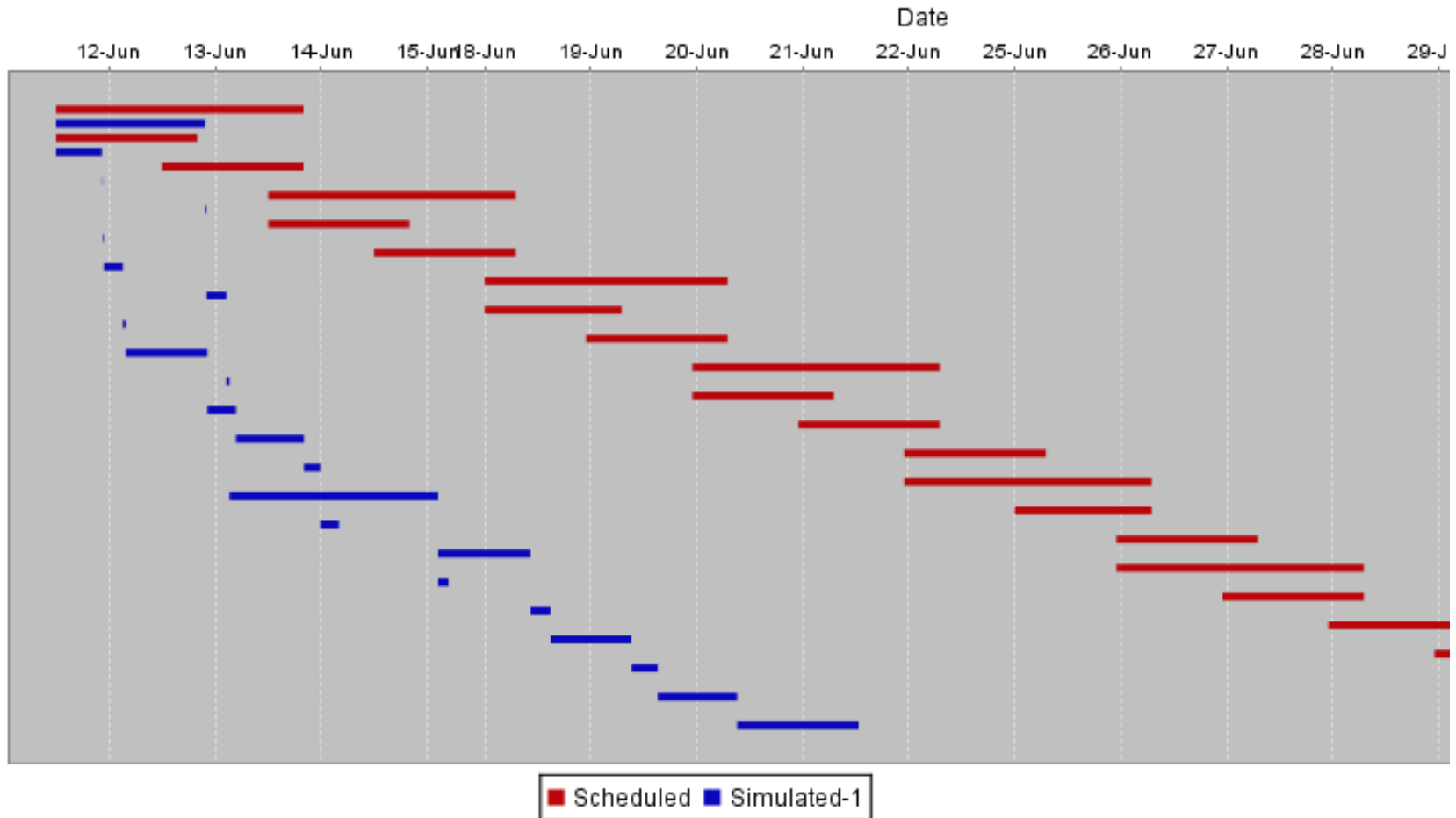


Simulation – Execution



- During execution of the plan, events and deviations can occur and may force the system to react
- Depending on the severity, the agents might have to reschedule, reassign, or even completely replan the remaining project

Demonstrator- Simulation Result



- Events can disturb the normal course of the project
 - People getting unavailable (sickness, vacation, leaving)
 - Resources failures (hardware crashes, tool bugs...)
 - Specification Changes (very common!)
 - Changes in Complexity
- Activity lengths can vary even without larger events
- Add actual events for correct analysis of past project
- Add random events for analysis of future projects

Assessment

- Analyze acquired data extended by the result of the simulation
- Gain KPIs for every part of the design process and point to possible problems
- Detailed effort reports:
 - development
 - debugging
 - verification
 - communication
 - setup
 - wasted effort

Assessment – “What-If” Predictions

- Change parameters of the design system and re-simulate to estimate effects
- “How will my performance change, if I”
 - “... invest in new computing equipment?”
 - “... buy new Tools?”
 - “... send my employees to trainings?”
 - “... hire new employees?”
- “What if I change the design methodology?”
- “How will I perform when switching to a smaller technology?”

Assessment – Stability Analysis

- add typical random events to simulation
- randomly vary activity lengths using a beta distribution
- Run a whole set of simulations to estimate robustness
- Analyze outliers for possible weak spots

Conclusions & Future Work

- So far our approach can handle all requirements
- First test cases are promising
- A large set of analyses are possible, even predictions (precision unknown so far)

- Project not complete yet
- Important aspects of the design systems are not modeled yet, behavioral part still in the beginning
- Setup effort is still unknown

The logo for VCAD, featuring a red 'V' followed by 'CAD' in black. The letters are bold and sans-serif. A red vertical bar is positioned above the 'V' and another below the 'D'.

VCAD