

Articulation and Sharing of Distributed Design Project and Process Knowledge

a short paper



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Tangier, Morocco, September 16, 2010

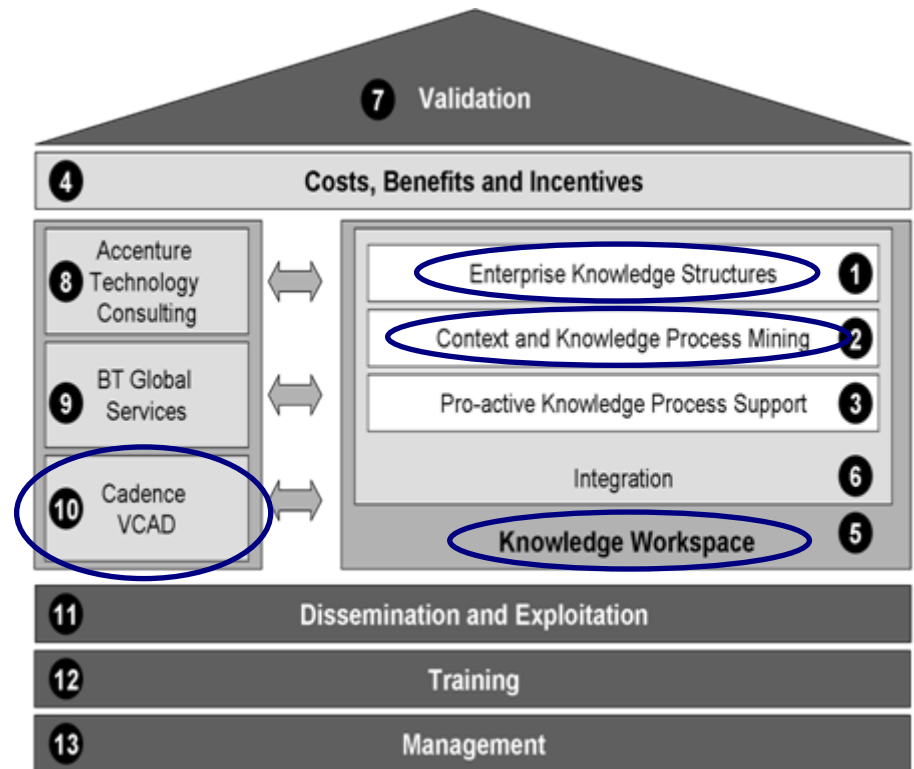
IDC 2010

Agenda

- ▶ Accent pretty much on what is not in the paper
- ...
- ▶ Research in the context of ACTIVE IP
 - Case Study – focus on performance management (informal processes)
- ▶ Approach and Prototype Architecture
- ▶ Implementation Results
- ▶ Knowledge Representation
- ▶ Summary

ACTIVE Integrated Project (FP7)

- ▶ Aim:
 - Increasing the productivity of knowledge workers in a pro-active, contextualized, yet easy and unobtrusive way
- ▶ Approach:
 - Convert tacit and unshared knowledge – the "hidden intelligence" of enterprises – into transferable, interoperable and actionable knowledge to support seamless collaboration and to enable problem solving
- ▶ Focus:
 - Productivity in informal processes



ACTIVE: Informal Processes

- ▶ Informal processes are carried out by knowledge workers with their skills, experience and knowledge, often to perform difficult tasks which require complex, informal decisions among multiple possible strategies to fulfill specific goals
- ▶ In contrast to business processes which are formal, standardized, and repeatable, knowledge processes are often not even written down, let alone denoted formally, vary from person to person to achieve the same objective, and are often not repeatable
- ▶ Knowledge workers create informal processes on the fly in many situations of their daily work

Cadence Design Systems

- ▶ A leader on the Electronic Design Automation (EDA) Market
- ▶ Customers:
 - Systems companies
 - Semiconductor companies
 - Design/supply chain partners
- ▶ Focus:
 - In Development – electronic systems and Integrated Circuits (IC's)
 - In Services: improving the productivity of our customers' design environments
- ▶ Cadence Global Services

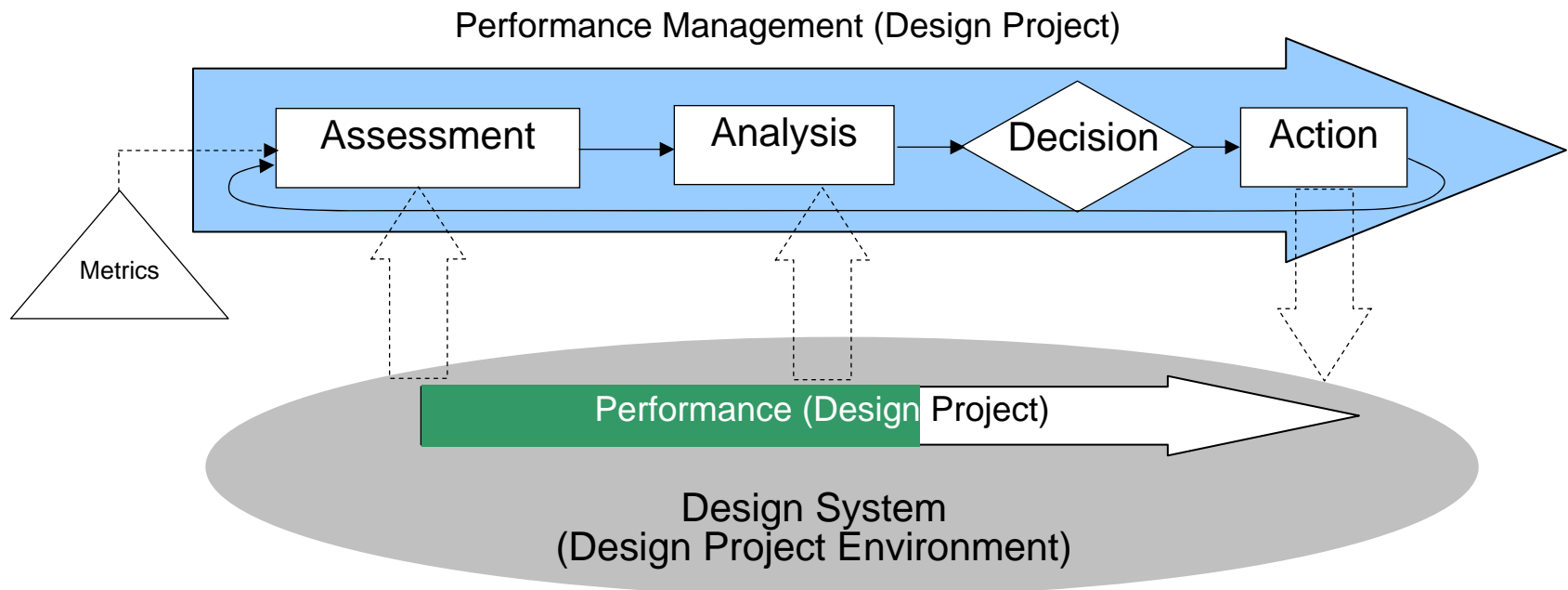


Informal Processes in MIC Design



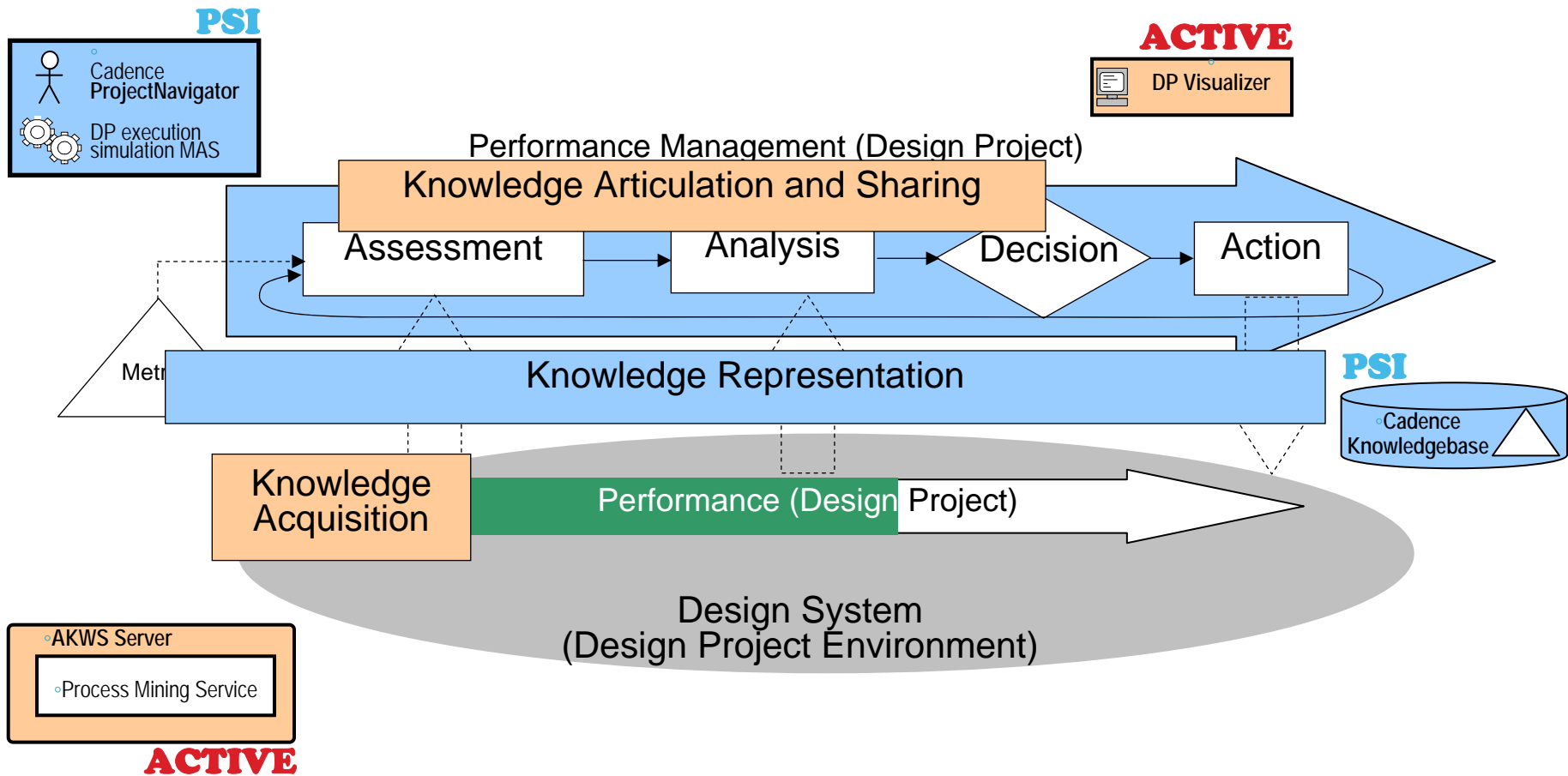
Performance Management

– an Informal Process

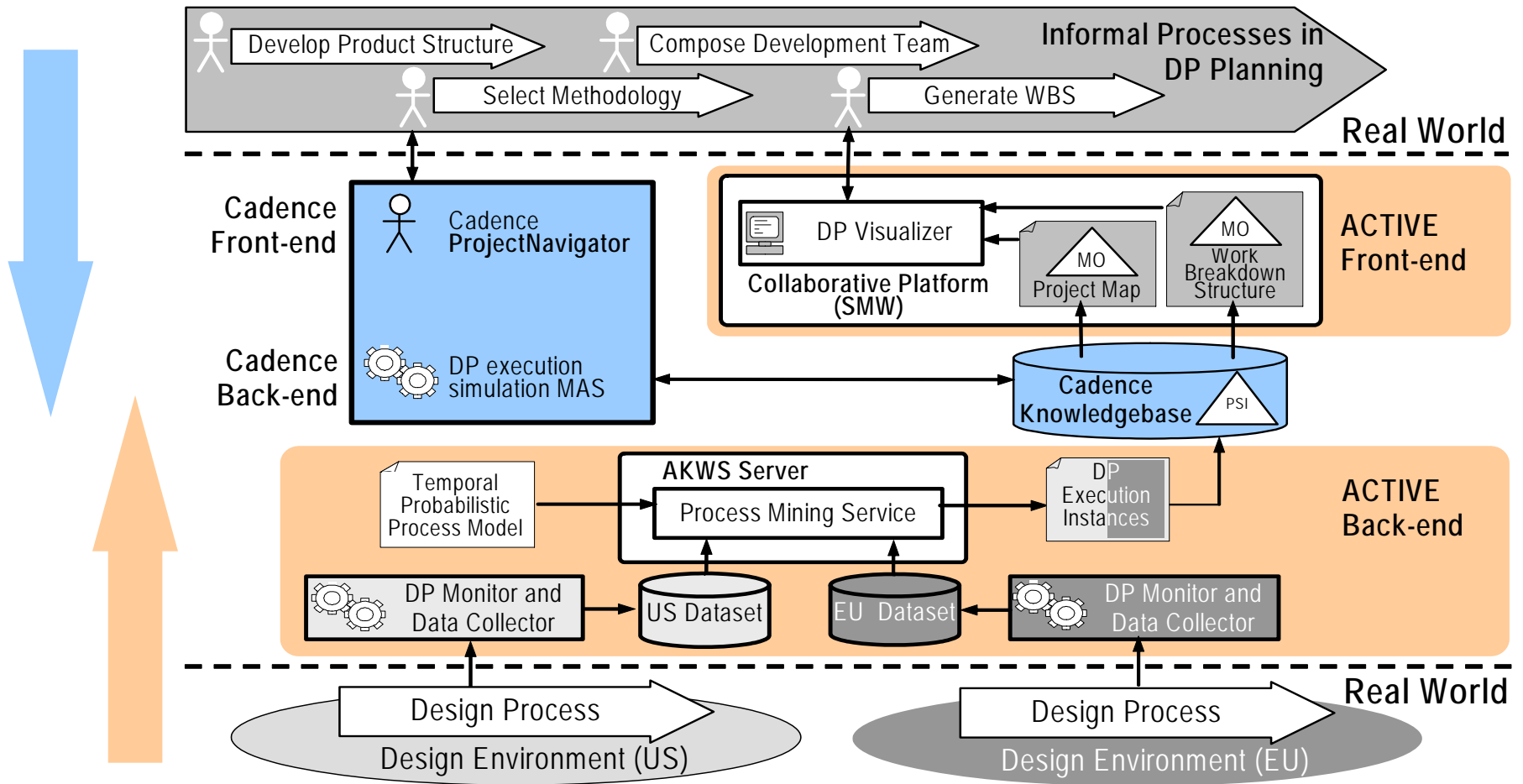


Performance Management

– an Informal Process



Prototype Architecture



↓ Develop Product Structure

Knowledge Articulation and Sharing in DP Visualizer

▶ Visualization

- Links to:
 - Processes
 - Tools
 - Actors

▶ Discussion

- Pro-con summaries
- Discussion threads

▶ LiveNetLife

- Page sharing and chats

The screenshot displays the DP Visualizer web application interface. The top part shows a hierarchical diagram of a product structure. The root node is 'pll Analog'. It has three child nodes: 'pll lf Analog' (with a change of +2,-1), 'pll iqdiv2 Analog' (with a change of +0,-0), and 'pll cp Analog' (with a change of +1,-0). A blue arrow points from the 'pll lf Analog' node to a discussion thread below.

The discussion thread is titled 'Talk:Http://psi.vcad-vlab.net/inst/project/tc1?DesignArtifact AEE90812A22CA3DD8'. It contains a table of comments:

Comment	User	Role	Status	ProCon	Text
DA Comment5	Vadim Ermolayev	KE	Minor	Pro	So far So Good
DA Comment8	Eyck Jentzsch	Project Manager	Major	Pro	Correspondence to Req Spec
DA Comment10	Wolf-Ekkehard Matzke	Lead Designer (Analog)	Major	Contra	Analog part insufficiently detailed

Below the table is a section titled 'Functional Block Structure' with the text: 'The structure of the analog part needs to be further elaborated'. At the bottom right, there is a chat window for 'Vadim Ermolayev' with a 'LIVENETLIFE' logo.

Select Development Methodology

and Bind it to the Product Structure

The screenshot shows a web browser window with the URL <http://psi.vcad-vlab.net/inst/kb/ds/cdns?GenericTask2>. The page displays a hierarchical diagram on the left with nodes for 'Analog Floorplanning', 'MasterTask of tc1', and 'Analog Layout'. On the right, there is a detailed information panel for 'Analog Floorplanning' with the following sections:

- Version:** 1
- Successors:** Analog Layout
- InputConfig:**
 - Http://psi.vcad-vlab.net/inst/kb/ds/cdns?InputConfig6
 - Http://psi.vcad-vlab.net/inst/kb/ds/cdns?InputConfig5
 - Http://psi.vcad-vlab.net/inst/kb/ds/cdns?InputConfig7
- OutgoingStatePattern:** Floorplan of Analog
- Roles:** Analog Frontend Designer
- Tools:** Virtuoso
- Tasks:** Analog Floorplanning of pll cp, Analog Floorplanning of pll, Analog Floorplanning of pll tqdiv2

At the bottom, it indicates 'Category: GenericTask'.

Generic

The screenshot shows a web browser window with the URL <http://psi.vcad-vlab.net/inst/project/tc1?Task1>. The page displays a complex flowchart diagram representing a task structure. The flow starts with a 'Start' node, leading to 'Analog Floorplanning of pll', which then branches into 'Analog Floorplanning of pll cp' and 'Analog Floorplanning of pll tqdiv2'. These further lead to various 'Analog Layout of pll' nodes, eventually converging to a 'Task' node. On the right, there is a metadata box for 'Analog Floorplanning of pll' with the following details:

- belongs to:** GenericTask: tc1
- Version:** 1
- has Actor:** Christoph
- has DA:** PG
- Tools:** Virtuoso

At the bottom, it indicates 'Category: Task'.

Product-Bound

Develop Work Breakdown Structure and Monitor Project Execution

Page Discussion

Read Edit View history

Go Search

Http://psi.vcad-vlab.net/inst/project/tc1?Task F9AA6612A22CA4104

	Resource	Duration	% Comp.	Start Date	End Date
- Design of pll	Christoph	104 Hours	100%	1/2/06	1/6/06
Analog Floorplanning of pll	Christoph	2 Hours	100%	1/2/06	1/2/06
Analog Floorplanning of pll_cp	Christoph	3 Hours	100%	1/2/06	1/2/06
Analog Floorplanning of pll_iqdiv2	Christoph	3 Hours	100%	1/2/06	1/2/06
Analog Layout of pll_cp_dni	Christoph	1 Hour	100%	1/2/06	1/2/06
Analog Layout of pll_cp_iqgen	Christoph	1 Hour	100%	1/3/06	1/3/06
Analog Layout of pll_cp	Christoph	1 Hour	100%	1/4/06	1/4/06
Analog Layout of pll_iqdiv2	Christoph	1 Hour	100%	1/4/06	1/4/06
Analog Layout of pll_tf	Christoph	1 Hour	100%	1/4/06	1/4/06
Analog Layout of pll	Christoph	1 Hour	100%	1/6/06	1/6/06

Powered by jsGantt Format: Hour Day Week Month

Design of pll

belongs to: Design

GenericTask: Design

Version: 1

has Actor: Christoph

has DA: pll

Planned Start Date: 01-Jan-2006 00:00:00

Planned Finish Date: 05-Jan-2006 11:00:00

Tools

Virtuoso

[MS Project XML export](#)

[Back to all Cadence processes](#)

Category: Task

This page was last modified on 23 August 2010, at 20:11.

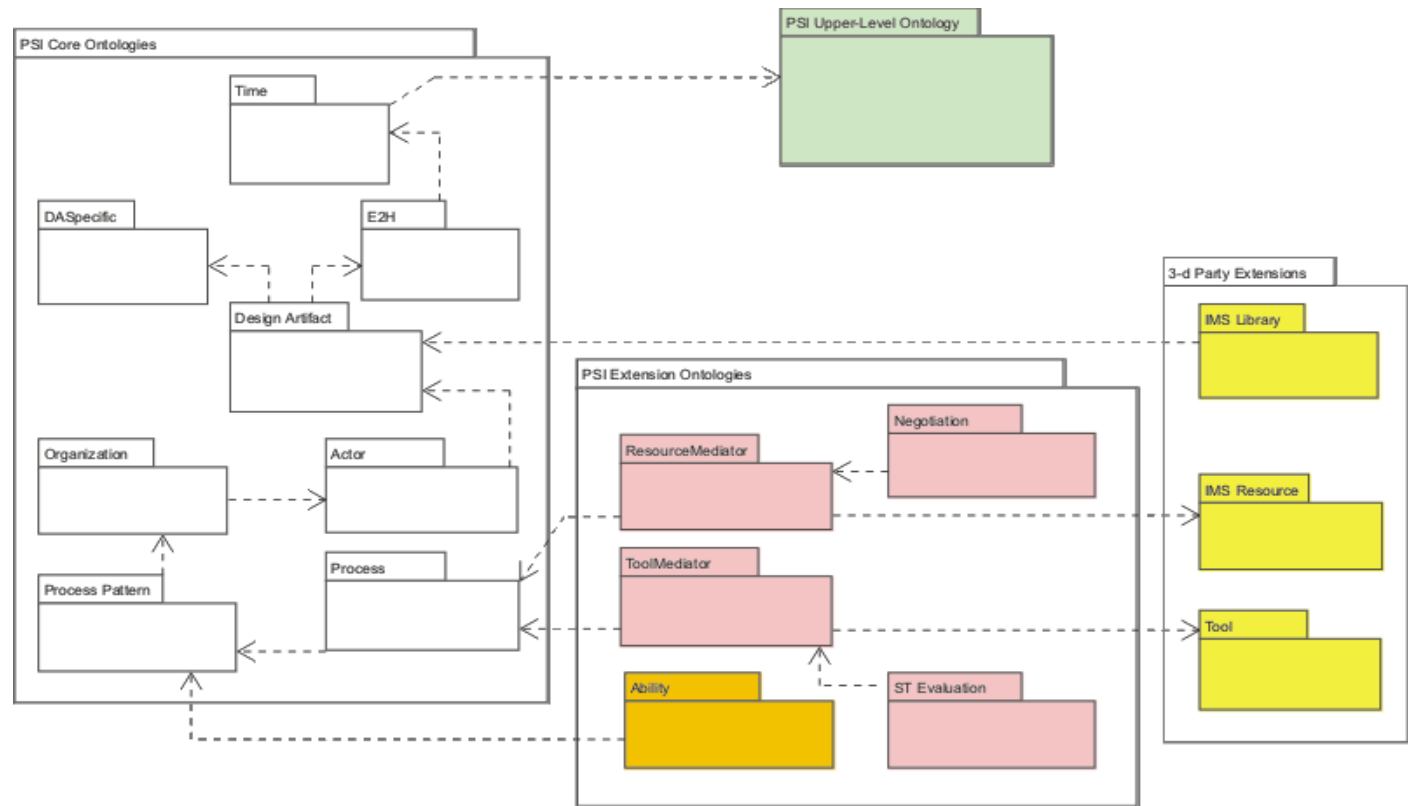
This page has been accessed 10 times.

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Vadim Ermolayev: [<enter chat here>](#)
<http://psi.vcad-vlab.net/inst/project/tc1> **LIVENETLIFE**

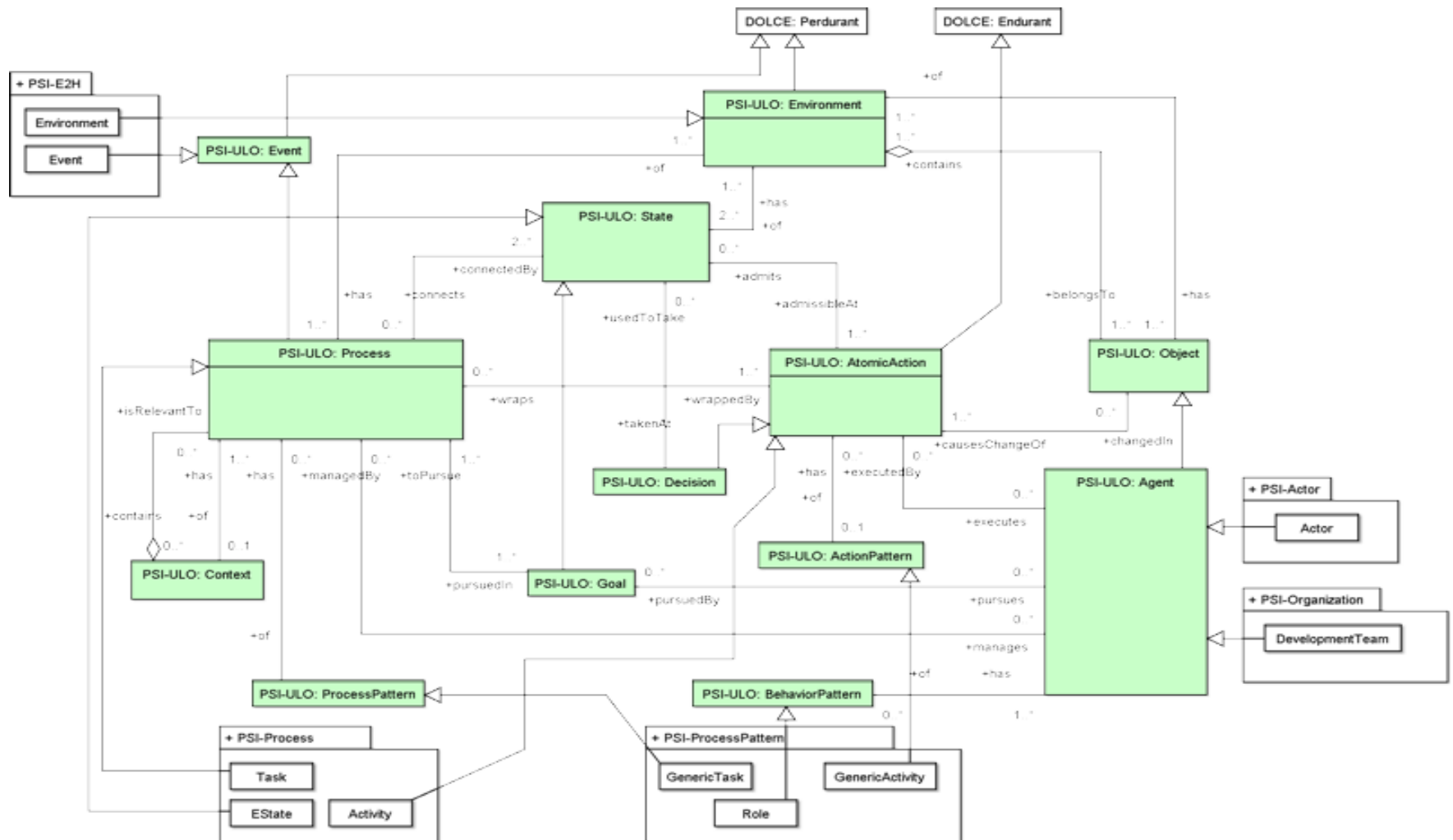
Knowledge Representation

- ▶ PSI Suite of Ontologies v.2.3
- ▶ OWL-DL

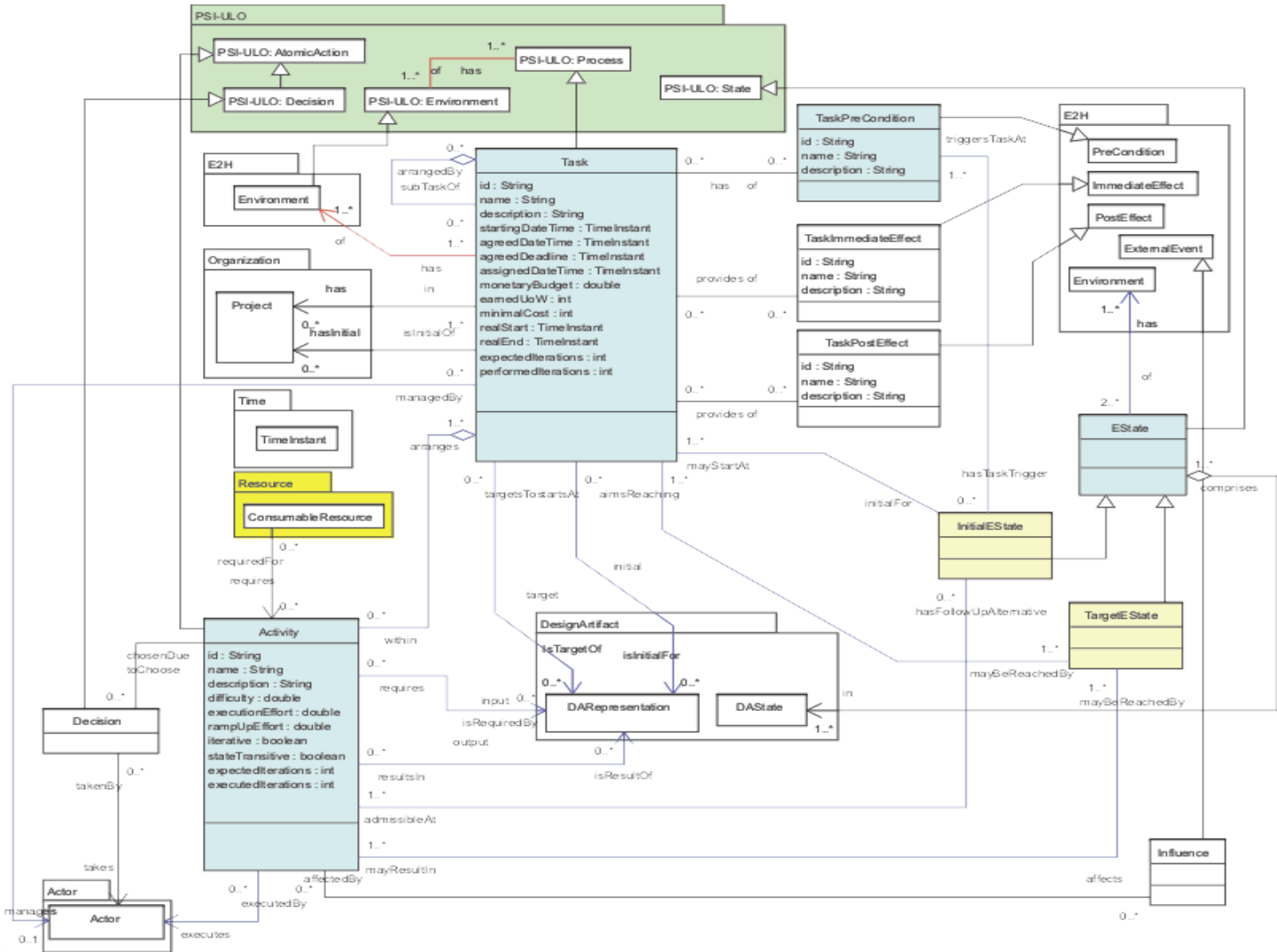


- ▶ [http://isrg.kit.znu.edu.ua/ontodocwiki/index.php/PSI Suite of Ontologies](http://isrg.kit.znu.edu.ua/ontodocwiki/index.php/PSI_Suite_of_Ontologies)

KR: PSI-ULO – Process Context



KR: PSI-Core Process Ontology



Summary

- ▶ Tacit (and distributed) knowledge acquisition articulation and sharing in MIC Engineering Design Projects
- ▶ Back-End: ACTIVE Knowledge WorkSpace
- ▶ Front-End: ACTIVE Design Project Visualizer
 - Paper – Demonstrator Prototype
 - Currently – Fully Functional Prototype
 - E.g. (front-end) Gantt chart visualization for WBS, execution monitoring, ...
- ▶ Planned future work (short term):
 - Validation with industrial users

Questions Please ...

